**Asynchronous Serial Interface**

During the first lab a simple test vector was generated to test the basic functionality of the circuit. There was a slight confusion regarding the 3X oversampling, but this was fixed, and test vector successfully passed the original Verilog model generated by the schematic. This test vector was then included in the final draft.

The final draft which was submitted included three test vectors. The first one clocked a single sequence of alternating 1’s and 0’s just to check if iLoad is going high when expected.

The second sequence was a test of the circuits state clocking, 3 different tests were included in this sequence. These tests were based on the ASM chart for this circuit. The first section was a test to see if the circuit responds correctly to an idle bit of 1. If iLoad is asserted 3 clock cycles earlier than defined in theses vectors, the circuit isn’t reliant on the start bit. The second one tests the circuits response to a new transmission occurring immediately after the previous one has concluded. The third one tests the circuit when a couple of idle bits occur between the old transition and the new one.

The third sequence was a test of the timing of the circuit. No clock signals are used, and the clock is administered manually with 1 and 0 bits to allow more accurate analysis to occur and to allow a more thorough test to be carried out within a clock cycle. The bit samples should be taken on the second rising edge from the clock.

During the 2nd lab all of the test vectors were inputted to the chip. After running the tests, there was a large number of errors shown – 146 to be exact. But this error count changed every time the test vectors were re-run, so it is unclear if there is an issue with the software or not.